REMARKS

This application, which is one of a series of related applications, discloses the processing of storage packets for, *inter alia*, virtualization, packet classification, and protocol translation at wire speed and without buffering by a storage switch which routes the packets between servers and physical storage targets in a storage network (see paragraph [0016], pg. 6). The invention claimed in this particular application concerns the virtualization of storage packets.

As defined in the specification, and as used in the claims, the term "virtualization" means the mapping of virtual target space to physical target space, and the conversion of a virtual target address to a physical target address, or vice versa (see paragraph [0063], pg. 14 and paragraph [0127], pg. 33).

This application contains independent Claims 1, 9, 10, 12, 14, 19, 24, 28, 29, 30, 31, 32 and 34. With the exception of Claims 19-23 which have been allowed, all claims have been rejected under 35 U.S.C. §103 on various combinations of U.S. Patent No. 6,400,730 to Latif, U.S. Patent No. 7,330,892 to Ibrahim, and U.S. Patent No. 6,735,198 to Edsall.

For the reasons set out below, it is submitted that none of these references, individually or in combination, teaches or suggests the invention set out in the rejected claims, and that they cannot render any of the claims unpatentable under 35 U.S.C. §103. It is further submitted that the Office's proposed combinations of the references are improper and that no logical combination of the references would produce the

claimed invention absent impermissible hindsight modification and reconstruction of both the structure and the functioning of the references, contrary to *KSR v. Teleflex,* 550 U.S. 398, 82 USPQ 2d 1385 (2007).

Accordingly, the various rejections of the claims under 35 U.S.C. §103 are traversed. It is submitted that these rejections are improper and should be withdrawn.

The Rejections Under 35 U.S.C. §103

As an initial matter, it is pointed out that obviousness under Section 103 requires that a claim, properly interpreted, be considered as a whole, and that the prior art would have rendered the claimed subject matter as a whole obvious to one of ordinary skill in the art at the time of the invention.

As pointed out by the Supreme Court in *KSR v. Teleflex*, *supra*, obviousness cannot be proved by merely demonstrating that each of the elements of the invention was independently known in the prior art. Rather, to show obviousness, one skilled in the art at the time of the invention must have appreciated from the prior art that the disclosed prior art elements were capable of being combined in the manner claimed, without changes in their respective functions, and that the combinations would have predictable yielded the claimed invention.

Here, while there may be some similarities between some claims and cited references, the elements of Latif, Ibrahim and Edsall could not have been combined in the manner proposed in the rejections, with no change in their respective functions,

and predictably yielded the claimed invention. Thus, for the reasons explained in detail below, the references cannot render the claimed invention obvious.

Claims 1, 2, 9, 30 and 31

The rejections of Claims 1, 2, 9, 30, and 31 as obvious and unpatentable over Latif in view of Ibrahim are traversed.

Independent Claim 1 is representative. It is directed to a method for routing packets between servers and physical storage targets by a storage switch in a storage network, and the claim recites, in relevant part:

> (a) receiving at a first port of the switch a packet that specifies as a destination a virtual storage target provisioned on a physical storage target;
>
> (b) sending at a second port of the switch the packet to said physical storage target; and
>
> wherein said sending comprises virtualizing said packet by translating a first address of said virtual storage target to a second address of said physical storage target without buffering the packet (*emphasis added)*

Independent Claim 9, and dependent Claim 2, are directed to a method similar to Claim 1, except that they recite that the virtualizing occurs at wire speed rather than without buffering the packet.

Latif relates to switching and transferring frames having non-compatible protocols (Fibre Channel (FC), SCSI, IP and Ethernet) between different devices in a network. The reference discloses encapsulating non-compatible frames into a local format for routing through the switch, which performs address translation between domains for the different frames. Even accepting for purposes of argument only the Office's position that address translation of a destination FC address and an IP

address is equivalent to virtualization, which is expressly disputed, Latif does not disclose or suggest that such address translation is done either without buffering a packet (as set out in Claim 1) or at wire speed (as recited in Claims 2 and 9), as correctly recognized by the Office. Moreover, neither of the other cited references discloses this.

The Office is incorrect in interpreting Ibrahim as teaching virtualization of a packet without buffering or at wire speed (see, e.g., Office Action pg. 4). Rather, Ibrahim, in fact, teaches that virtualization and resolution of contentions and granting of permission for access to a device to establish a data path through the controller is not performed at wire speed or without buffering. Ibrahim actually discloses that once a data channel is established through the virtualization controller after performing the required address mappings (virtualization) and resolving contentions, only then does the controller allow data transfers over the established channel between the host and the storage device to occur at wire speed (col.4, lns. 59-63).

Ibrahim does not teach performing virtualization at wire speed (Claims 2 and 9), or without buffering (Claim 1). To the contrary, Ibrahim expressly teaches that the controller (302, Fig. 3) is adapted for establishing a connection between a selected upstream processing element (UPE) (304, 306) and a host (308, 310) for transferring data between the host and its corresponding VLUN by configurably and intermittently coupling to an associated downstream processing element (DPE) (312, 314) to form a data channel 324 that is exclusive for the time period required to transfer a slice of data, and that the "channel 324 is operable at wire speed" (see col. 4, ln. 64 – col. 5,

ln. 20). Ibrahim only teaches that data transfer through the established channel occurs at "wire speed". Performing the address mappings and obtaining the permissions to establish the channel do not.

Ibrahim discloses explicitly that the term "wire speed means that the data transfers occur at a rate that matches the data rate of the link to which the storage virtualization controller is connected . . ." (*emphasis added*) (col. 5, lns 21-23). Ibrahim does not either state or imply that virtualization occurs at wire speed, but rather that only data transfers over an established channel occur at wire speed.

Additionally, Ibrahim also describes (at col. 7, lns 14-24) the operation of the controller in processing a read, write or status command. The reference states that a command processor 332 in the controller requests permission from a CPE for exclusive access to a storage device, and that once permission is received, the UPE 304 may engage in wire speed communications with the selected DPE 314. Subsequently received data frames also are transferred between the UPE and the DPE at wire speed. This clearly discloses that only after a connection is established between an UPE and a DPE does data transfers occur at wire speed.

Ibrahim further confirms that virtualization does not occur at wire speed in his description (between col. 8, ln. 35 – col. 9, ln. 30) of the operation of the virtualization controller illustrated in Figure 4. Ibrahim makes clear (see col. 8, lns. 61-66) that in step 412 of Figure 4, data is transferred between the UPE and the DPE "at substantially a rated speed of the storage network after permission is obtained and the method [of establishing the connection] concludes" (*emphasis added).*

Thus, it is clear that Ibrahim does not teach either that the virtualization process or the process for requesting and being granted permission to access a storage device occurs at wire speed or without buffering. Accordingly, Ibrahim in combination with Latif cannot render Claims 1, 2 and 9 obvious.

If the Examiner's statement with reference to Figure 3 that "the elements within 302 have no need for a buffer" (see e.g., Office Action, page 4) is intended to indicate a teaching in the reference of "without buffering" to support his rejection, it is respectfully pointed out that he is in error and has failed to establish a *prime facie* case for the rejection. The absence of a disclosure in a reference of a buffer teaches nothing. It does not equate to and does not mean that the reference affirmatively teaches or suggests a claim limitation "without buffering", and the absence of disclosure will not support a rejection. To establish a prima facie basis for the rejection, there must be an affirmative disclosure in a reference of no buffering or other factual basis demonstrating the absence of a buffer in the context of virtualization. The mere absence of any disclosure or showing of a buffer in a functional block diagram of the virtualization controller does not constitute a teaching or a conclusion that the controller functions without buffering, and will not provide the necessary factual basis to support a *prima facie* rejection.

Thus, the rejections under 35 U.S.C. §103 of Claims 1, 2 and 9 on Latif in view of Ibrahim are improper.

Claim 31:

Independent Claim 31 is directed to a linecard for a storage switch, and calls for a plurality of processors that each include a "wire-speed virtualization unit that translates a virtual target address . . . to a physical target address". The rejection of Claim 31 on Latif and Ibrahim is improper and is traversed for the same reasons set forth above with respect to Claims 1, 2 and 9. Ibrahim does not disclose a virtualization unit that either operates at wire speed to virtualize addresses, or that does so without buffering, as claimed, and Ibrahim in combination with Latif does not and cannot render the claim obvious for at least these same reasons.

Claims 30 and 32:

Independent Claim 30, which is also directed to a linecard, calls for "means for performing a virtualization function to translate a virtual target address . . . to a physical target address . . . without buffering". Independent Claim 32, which is directed to a switch, is similar in calling for "means for translating a virtual target address . . . to a physical target address . . . without buffering".

These claim elements are written in means plus function form, and must be interpreted pursuant to 35 U.S.C. §112, ¶6 to cover the structure, material and acts disclosed in the specification for performing the recited function, and equivalents thereof. (See also M.P.E.P. §2181 (8th ed., Rev.7, Jul. 2008). The Examiner has failed to do so. The burden is on the Office to show the same or equivalent structure in the Latif and Ibrahim references as that disclosed in the specification for performing the claimed virtualization function in order to support a rejection on these references.

Having failed to satisfy this burden, the rejections of Claims 30 and 32 are defective and improper for this reason alone.

Moreover, the rejections of Claims 30 and 32 on Latif and Ibrahim are improper and are traversed for the same reasons set forth above with respect to Claims 1, 2 and 9. The references do not in combination teach or suggest any structure for virtualization without buffering, much less structure equivalent to that disclosed in the specification for this purpose. Thus, the rejections of Claims 30 and 32 are improper for these reasons also.

Claims 3-8, 10-16, 18, 24-29 and 32-35

The rejections of Claims 3-8, 10-16, 18, 24-29 and 32-35, comprising independent Claims 10, 12, 14, 24, 29, 32 and 34, under 35 U.S.C. §103 as obvious over Latif in view of Ibrahim and in view of Edsall are traversed.

Independent Claims 10, 12, 14, 24, 29, 32 and 34 are directed to methods, storage switches, and storage media storing software instructions for execution by a processor for virtualizing and routing packets between servers and physical targets in a storage network. While these claims include different limitations, and have different degrees of specificity in their recitations, they all require virtualization of packets to be either without buffering or at wire speed.

As discussed above, Latif and Ibrahim do not individually or in combination teach or suggest virtualization of packets, either without buffering or at wire speed. Thus, for at least the reasons set out above, Latif and Ibrahim cannot support a

rejection of these independent claims or the claims dependent thereon for obviousness. Edsall does cure the deficiencies in the teachings of Latif and Ibrahim, and adds nothing to support the rejections.

Edsall discloses the updating and synchronizing of forwarding tables on line cards having ports interconnected by a switch fabric in a distributed network. However, contrary to the Office's characterization of Edsall, the reference does not disclose or suggest virtualization of packets without buffering or at wire speed. In contrast, as pointed out below, Edsall expressly teaches the buffering of frames.

Edsall discloses linecards having a plurality of ports and forwarding tables for lookup of destinations for forwarding of frames. However, the teachings of Edsall are incompatible with the Examiner's interpretation of the teaching of Ibrahim as disclosing virtualization at wire speed or without buffering, and this incompatibility defeats the Examiner's proposed combination of Edsall with Ibrahim and Latif.

In particular, Edsall expressly discloses the "buffering of frames destined for the switch fabric" (col. 10, lns. 17-18) and the loading of incoming frames at a port into a "frame buffer associated with port interface circuitry" (col. 10, lns.47-48). Thus, Edsall teaches linecards having ports with buffers for buffering frames arriving at a switch port and being routed through the switch using the routing tables, which is contrary and opposite to the Examiner's interpretation of Ibrahim as disclosing virtualization at wire speed without buffering. Therefore, the Examiner is basing his rejections on proposed combinations of references having incompatible teachings. The references cannot be combined as proposed, and will not support the rejections, absent

reconstruction of the references using the hindsight afforded by the present specification.

Thus, the proposed combination of the references will not support the rejections of Claims 3-8, 10-16, 18, 24-29 and 32-35 based upon Latif, Ibrahim and Edsall, and the rejections are improper.

It is respectfully submitted that the cited prior art cannot be combined in the ways suggested by the Office, and that this prior art does not teach or suggest a method for use in a storage switch, a storage switch, a linecard for a storage switch, or a method preformed by a processor in a storage switch executing software instructions, as claimed. Accordingly, this prior art cannot render the claims obvious and unpatentable.

In view of the foregoing, it is respectfully submitted that all rejections have been overcome and that this application is in condition for allowance. Accordingly, favorable reconsideration of this application is requested, and early allowance of all claims is solicited.

In accordance with the duty of disclosure, Applicants calls to the attention of the Examiner that the Board of Patent Appeals and Interferences affirmed in part a rejection of claims based upon the Latif and Tzeng references, of record herein, in U.S. Application 10/051,321, a related application to the present application referenced in paragraph [0002] of this application (see Appeal 2008-003917). The

rejected claims, while similar in some respects to the present claims, were directed to different subject matter.

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Respectfully Submitted,

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